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EXAMINER	
ABRISHAMKAR, KAVEH	
ART UNIT	**PAPER NUMBER**
2131	

DATE MAILED: 05/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/479,105	ROCHE, FRANCK	
	Examiner	Art Unit	
	Kaveh Abrishamkar	2131	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 December 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *10-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *10-42* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This action is in response to the amendment filed on December 20, 2004. The original application contained claims 10 – 42. No claims have been amended, cancelled or added. Presently pending claims are 10-42.

Response to Arguments

2. Applicant's arguments received on December 20, 2004, have been fully considered but are not persuasive for the following reasons:

Regarding independent claim 10, the applicant argues that the CPA, Banno et al. (U.S. Patent No. 5,680,581), does not that access to the internal memory is blocked after each resetting of the microprocessor. This argument is not found persuasive. The CPA states that "the contents of the internal memory cannot be read out using an instruction stored in a memory outside the address space of the internal program memory, and can be prevented from being disclosed to a third party" (column 6 line 65 – column 7 line 2). This access prevention to the internal memory will be maintained as long as the address is not in the address space of the program memory, and therefore, access is blocked to internal memory after and before a resetting of the microprocessor, unless the address (password) matches with the address in the address space of the internal program memory. The applicant further argues that the CPA does not teach that the protection circuit is released by a successive sending on the data bus of N

passwords proper to the register. This argument is not found persuasive. The CPA discloses that "an address decoder receives an address (password) transferred from the address bus, detects if the received address (password) is present in the address space (proper to register)" (column 4 lines 47-61), and if it is, the protection circuit is released. The password disclosed by the applicant are interpreted as a stream of bits that must match previously stored data in order to release the protection circuit, which is what the CPA discloses.

Accordingly, the rejection for the pending claims 1-42 is respectfully maintained as given below.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 10 – 15, 17 – 22, 24 – 32, and 35 – 42 are rejected under 35 U.S.C. 102(b) as being anticipated by Banno et al. (U.S. Patent 5,680,581).

Regarding claim 1, Banno discloses:

A microprocessor comprising:

an address bus (Figure 1 item 15, column 4 lines 48 – 55);

a data bus (Figure 1 item 16, column 4 lines 48 – 55);

a plurality of read and write accessible registers connected to said data bus (column 4 lines 48 – 55);

an address decoder connected to said address bus for selecting said plurality of registers as a function of an address provided by said address bus (Figure 2, item 12a); and

a plurality of protection circuits connected between said address decoder and said plurality of registers, each protection circuit associated with a register to secure access thereto by blocking selection of said register after each resetting of the microprocessor, and releasing of said protection circuit by a successive sending on said data bus of N passwords proper to said register during N first operations for selection of said register with $N \geq 1$, the selection of said associated register being effective only for subsequent operations for the selection thereof until a next resetting of the microprocessor (Figure 1 item 12, column 4 line 47 – column 5 line 48).

Regarding claim 19, Banno discloses:

A microprocessor comprising:

an address bus (Figure 1 item 15, column 4 lines 48 – 55);

a data bus (Figure 1 item 16, column 4 lines 48 – 55);

a plurality of read and write accessible registers connected to said data bus (column 4 lines 48 – 55);

an address decoder connected to said address bus for selecting said plurality of registers as a function of an address provided by said address bus (Figure 2, item 12a); and

a plurality of protection circuits connected between said address decoder and said plurality of registers, each protection circuit associated with a register to secure access thereto by blocking selection of said register during write access operations after each resetting of the microprocessor, and releasing of said protection circuit by a successive sending on said data bus of N passwords proper to said register during N first operations for selection of said register with $N \geq 1$, the selection of said associated register being effective only for subsequent operations for the selection thereof until a next resetting of the microprocessor (Figure 1 item 12, column 4 line 47 – column 5 line 48).

Regarding claim 26, Banno discloses:

A microprocessor comprising:

an address bus (Figure 1 item 15, column 4 lines 48 – 55);

a data bus (Figure 1 item 16, column 4 lines 48 – 55);

a plurality of read and write accessible registers connected to said data bus (column 4 lines 48 – 55);

an address decoder connected to said address bus for selecting said plurality of registers as a function of an address provided by said address bus (Figure 2, item 12a); and

a plurality of protection circuits connected between said address decoder and said plurality of registers (Figure 1 item 12, column 4 line 47 – column 5 line 48);

each protection circuit associated with a register to secure access thereto by blocking selection of said register after each resetting of the microprocessor, at least two passwords are provided to each register, and releasing of said protection circuit by a successive sending on said data bus of at least 2N passwords proper to said register during N first operations for selection of said register with $N \geq 1$, the selection of said associated register being effective only for subsequent operations for the selection thereof until a next resetting of the microprocessor (Figure 1 item 12, column 4 line 47 – column 5 line 48).

Regarding claim 37, Banno discloses:

A method for securing access to a plurality of registers of a microprocessor, the method comprising the steps of:

selecting one of said plurality of registers via an address decoder as a function of an address provided by an address bus connected to the address decoder (Figure 2, item 12a);

blocking selection of the plurality of registers via a plurality of protection circuits after each resetting of the microprocessor (Figure 1 item 12, column 4 line 47 – column 5 line 48); and

releasing a protection circuit associated with a selected register by successive sending on the data bus N passwords proper to the selected register during N first

operations for selection of the register with N ≥ 1, the selection of the register being effective only for subsequent operations for the selection thereof until a next resetting of the microprocessor (Figure 1 item 12, column 4 line 47 – column 5 line 48).

Claim 11 is rejected as applied above in rejecting claim 10. Furthermore, Banno discloses:

A microprocessor according to claim 10, wherein each protection circuit is arranged to block the selection of said associated register during read and write access operations to said associated register after each resetting of the microprocessor (Figure 1 item 12, Figure 4 item 22, column 5 lines 1 – 4).

Claim 12 is rejected as applied above in rejecting claim 10. Furthermore, Banno discloses:

A microprocessor according to claim 10, wherein each protection circuit is arranged to block the selection of said associated register during write access operations to said associated register after each resetting of the microprocessor (Figure 1 item 12, Figure 4 item 22, column 5 lines 1 – 4).

Claim 13 is rejected as applied above in rejecting claim 10. Furthermore, Banno discloses:

A microprocessor according to claim 10, wherein each protection circuit is connected between an output of said address decoder and a selection input of said

associated register for selection thereof (Figure 1 item 12, Figure 4 item 22, column 5 lines 1 – 4).

Claim 14 is rejected as applied above in rejecting claim 10. Furthermore, Banno discloses:

A microprocessor according to claim 10, wherein each protection circuit, during the first N operations for the selection of said associated register, compare N data elements present on said data bus with the N passwords proper to said associated register, and each protection circuit is released for subsequent operations of selection of said associated register until the next resetting of the microprocessor if the N data elements correspond to the N passwords (Figure 1 item 12, column 4 lines 45 – column 5 line 48).

Clam 15 is rejected as applied above in rejecting claim 10. Furthermore, Banno discloses:

A microprocessor according to claim 10, wherein a single password is provided for each register (column 5 lines 1 – 48); and wherein each protection circuit comprises:

a comparator circuit for comparing, during a first operation for the selection of said register, a data element present on said data bus with the password proper to said register and for delivery of an output signal representing a result of the comparison (column 5 lines 1 – 48);

first means for holding in each protection circuit the output signal until the next resetting of the microprocessor (column 4 lines 52 – 61); and

second means permitting the selection of said register if the output signal indicates that the data present on said data bus during the first operation of selection of said register corresponds to the password associated with said register (column 5 lines 32 – 48).

Claim 20 is rejected as applied above in rejecting claim 19. Furthermore, Banno discloses:

A microprocessor according to claim 19, wherein each protection circuit is connected between an output of said address decoder and a selection input of said associated register for selection thereof (Figure 1 item 12, Figure 4 item 22, column 5 lines 1 – 4).

Claim 21 is rejected as applied above in rejecting claim 19. Furthermore, Banno discloses:

A microprocessor according to claim 19, wherein each protection circuit, during the first N operations for the selection of said associated register, compares N data elements present on said data bus with the N passwords proper to said associated register, and each protection circuit is released for subsequent operations of selection of said associated register until the next resetting of the microprocessor if the N data

elements correspond to the N passwords (Figure 1 item 12, column 4 line 45 – column 5 line 48).

Claim 22 is rejected as applied above in rejecting claim 19. Furthermore, Banno discloses:

A microprocessor according to claim 19, wherein a single password is provided for each register (column 5 lines 1 – 48); and wherein each protection circuit comprises:

a comparator circuit for comparing, during a first operation for the selection of said register, a data element present on said data bus with the password proper to said register and for delivery of an output signal representing a result of the comparison (column 5 lines 1 – 48);

first means for holding in each protection circuit the output signal until the next resetting of the microprocessor (column 4 lines 52 – 61); and

second means permitting the selection of said register if the output signal indicates that the data present on said data bus during the first operation of selection of said register corresponds to the password associated with said register (column 5 lines 32 – 48).

Claim 27 is rejected as applied above in rejecting claim 26. Furthermore, Banno discloses:

A microprocessor according to claim 26, wherein the at least two passwords for said associated register are provided over said data bus in a predetermined order (column 5 lines 1 – 48).

Claim 28 is rejected as applied above in rejecting claim 26. Furthermore, Banno discloses:

A microprocessor according to claim 26, wherein each protection circuit is arranged to block the selection of said associated register during read and write access operations to said associated register after each resetting of the microprocessor (Figure 1 item 12, Figure 4 item 22, column 5 lines 1 – 4).

Claim 29 is rejected as applied above in rejecting claim 26. Furthermore, Banno discloses:

A microprocessor according to claim 26, wherein each protection circuit is arranged to block the selection of said associated register during write access operations to said associated register after each resetting of the microprocessor (Figure 1 item 12, Figure 4 item 22, column 5 lines 1 – 4).

Claim 30 is rejected as applied above in rejecting claim 26. Furthermore, Banno discloses:

A microprocessor according to claim 26, wherein each protection circuit is connected between an output of said address decoder and a selection input of said

associated register for selection thereof (Figure 1 item 12, Figure 4 item 22, column 5 lines 1 – 4).

Claim 31 is rejected as applied above in rejecting claim 26. Furthermore, Banno discloses:

A microprocessor according to claim 26, wherein each protection circuit, during the first N operations for the selection of said associated register, compare at least 2N data elements present on said data bus with at least 2N passwords proper to said associated register, and each protection circuit is released for subsequent operations of selection of said associated register up to the next resetting of the microprocessor if the at least 2N data elements correspond to at least 2N passwords (Figure 1 item 12, column 4 line 45 – column 5 line 48).

Claim 32 is rejected as applied above in rejecting claim 26. Furthermore, Banno discloses:

A microprocessor according to claim 26, wherein each protection circuit comprises:

a first protection circuit portion comprising a first comparator circuit for comparing, during a first operation for the selection of said register, a data element present on said data bus with a first one the at least two passwords proper to said register and for delivery of an output signal representing a result of the comparison, and

first means for holding in each protection circuit the output signal until the next resetting of the microprocessor (column 4 line 45 – column 5 line 61); and

a second protection circuit portion connected to an output of said first protection circuit portion and comprising a second comparator circuit for comparing, during the first operation for the selection of said register, the data element present on said data bus with a second one of the at least two passwords proper to said register and for delivery of an output signal representing a result of the comparison (column 4 line 45 – column 5 line 61),

second means for holding in each protection circuit the output signal until the next resetting of the microprocessor(column 4 line 45 – column 5 line 61); and

third means permitting the selection of said register for the subsequent selection operations of said register if the output signal indicates that the data present on said data bus during the first operation of selection thereof corresponds to the at least two passwords associated with said register (column 4 line 45 – column 5 line 61).

Claim 38 is rejected as applied above in rejecting claim 37. Furthermore, Banno discloses:

A method according to claim 37, wherein the step of blocking comprises blocking selection of a selected register during read and write access operations to that register after each resetting of the microprocessor (column 5 lines 1 – 4).

Claim 39 is rejected as applied above in rejecting claim 37. Furthermore, Banno discloses:

A method according to claim 37, wherein the step of blocking comprises blocking selection of a selected register during write access operations to that register after each resetting of the microprocessor (column 5 lines 1 – 4).

Claim 40 is rejected as applied above in rejecting claim 37. Furthermore, Banno discloses:

A method according to claim 37, wherein each protection circuit is connected between an output of the address decoder and a selection input of an associated register for selection thereof (Figure 1 item 12, Figure 4 item 22, column 5 lines 1 – 4).

Claim 41 is rejected as applied above in rejecting claim 37. Furthermore, Banno discloses:

A method according to claim 37, wherein each protection circuit, during the first N operations for the selection of an associated register, compares N data elements present on the data bus with the N passwords proper to the associated register, and each protection circuit is released for subsequent operations of selection of the associated register until the next resetting of the microprocessor if the N data elements correspond to the N passwords (Figure 1 item 12, column 4 line 45 – column 5 line 48).

Claim 42 is rejected as applied above in rejecting claim 37. Furthermore, Banno discloses:

A method according to claim 37, wherein a single password is provided for each register; and wherein the steps of blocking and releasing comprise:

comparing, during a first operation for the selection of the register, a data element present on the data bus with the password proper to the register and for delivery of an output signal representing a result of the comparison (column 4 line 47 – column 5 line 48);

holding in each protection circuit the output signal until the next resetting of the microprocessor (column 4 line 47 – column 5 line 48); and

permitting the selection of the register for subsequent selection operations of the register if the output signal indicates that the data present on the data bus during the first operation of selection of the register corresponds to the password associated with the register (column 4 line 47 – column 5 line 48).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 16-18, 23-25, and 33 – 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Banno et al. (U.S. Patent 5,680,581) in view of Tokumatsu et al. (U.S. Patent 5,222,001).

Claim 16 is rejected as applied above in rejecting claim 15. Banno does not explicitly disclose the use of first and second type flip-flops as a first means to hold the output signal until the next resetting of the microprocessor. Tokumatsu discloses the use of flip-flops to store a strobe signal (output signal) (column 6 lines 20 – 30). Furthermore, Tokumatsu discloses a clock pulse (clock input) connected to the address decoder (column 8 lines 29 – 46). Tokumatsu further discusses the first latch circuit (first flip-flop circuit) being latched to a second latch circuit (second flip-flop) (column 6 lines 21 – 50). Banno and Tokumatsu are analogous arts because both pertain to transmitting instruction signals, and using an address decoder to determine accessibility to a memory element. Therefore, it would have been obvious of one of ordinary skill in the art at the time the Applicant's invention was made to replace the two-input AND gate provided by Banno to provide double-latching of the strobe signal (output signal) prior to the selection of the register via the AND gate.

Claim 23 is rejected as applied above in rejecting claim 22. Banno does not explicitly disclose the use of first and second type flip-flops as a first means to hold the output signal until the next resetting of the microprocessor. Tokumatsu discloses the use of flip-flops to store a strobe signal (output signal) (column 6 lines 20 – 30). Furthermore,

Tokumatsu discloses a clock pulse (clock input) connected to the address decoder (column 8 lines 29 – 46). Tokumatsu further discusses the first latch circuit (first flip-flop circuit) being latched to a second latch circuit (second flip-flop) (column 6 lines 21 – 50). Banno and Tokumatsu are analogous arts because both pertain to transmitting instruction signals, and using an address decoder to determine accessibility to a memory element. Therefore, it would have been obvious of one of ordinary skill in the art at the time the Applicant's invention was made to replace the two-input AND gate provided by Banno to provide double-latching of the strobe signal (output signal) prior to the selection of the register via the AND gate.

Claim 17 is rejected as applied above in rejecting claim 16. Furthermore, Banno discloses:

A microprocessor according to claim 16, wherein said second means comprises:

a delay circuit (Figure 2 item 12 c, column 4 line 47 – column 5 line 61);

a two-input AND logic gate having a first input connected to the output of said address decoder for selecting the register associated with said protection circuit, a second input connected through said delay circuit to the output of said second flip-flop circuit of first means, and an output connected to the selection input of said associated register (Figure 2 item 12c).

Claim 24 is rejected as applied above in rejecting claim 23. Furthermore, Banno discloses:

Claim 17 is rejected as applied above in rejecting claim 16. Furthermore, Banno discloses:

A microprocessor according to claim 16, wherein said second means comprises:

a delay circuit (Figure 2 item 12 c, column 4 line 47 – column 5 line 61);

a two-input AND logic gate having a first input connected to the output of said address decoder for selecting the register associated with said protection circuit, a second input connected through said delay circuit to the output of said second flip-flop circuit of first means (Figure 2 item 12c);

a second two-input AND logic gate having a first input connected to the output of said address decoder which has the task of selecting the register associated with said protection circuit, and a second input receiving a read/write signal column 4 line 47 – column 5 line 61); and

an OR logic gate having a first input connected to an output of said first two-input AND logic gate, and a second input connected to an output of said second two-input AND logic gate, and an output connected to said register column 4 line 47 – column 5 line 61).

Claim 33 is rejected as applied above in rejecting claim 32. Banno does not explicitly disclose the use of first and second type flip-flops as a first means to hold the output signal until the next resetting of the microprocessor. Tokumatsu discloses the use of flip-flops to store a strobe signal (output signal) (column 6 lines 20 – 30). Furthermore, Tokumatsu discloses a clock pulse (clock input) connected to the address decoder

(column 8 lines 29 – 46). Tokumatsu further discusses the first latch circuit (first flip-flop circuit) being latched to a second latch circuit (second flip-flop) (column 6 lines 21 – 50). Banno and Tokumatsu are analogous arts because both pertain to transmitting instruction signals, and using an address decoder to determine accessibility to a memory element. Therefore, it would have been obvious of one of ordinary skill in the art at the time the Applicant's invention was made to replace the two-input AND gate provided by Banno to provide double-latching of the strobe signal (output signal) prior to the selection of the register via the AND gate.

Claim 34 is rejected as applied above in rejecting claim 33. Banno does not explicitly disclose the use of first and second type flip-flops as a first means to hold the output signal until the next resetting of the microprocessor. Tokumatsu discloses the use of flip-flops to store a strobe signal (output signal) (column 6 lines 20 – 30). Furthermore, Tokumatsu discloses a clock pulse (clock input) connected to the address decoder (column 8 lines 29 – 46). Tokumatsu further discusses the first latch circuit (first flip-flop circuit) being latched to a second latch circuit (second flip-flop) (column 6 lines 21 – 50). Banno and Tokumatsu are analogous arts because both pertain to transmitting instruction signals, and using an address decoder to determine accessibility to a memory element. Therefore, it would have been obvious of one of ordinary skill in the art at the time the Applicant's invention was made to replace the two-input AND gate provided by Banno to provide double-latching of the strobe signal (output signal) prior to the selection of the register via the AND gate.

Claim 18 is rejected as applied above in rejecting claim 17. Furthermore, Banno discloses:

A microprocessor according to claim 17, wherein said delay circuit comprises a shift register synchronized with the operations for the selection of said associated register (column 4 line 47 – column 5 line 61).

Claim 25 is rejected as applied above in rejecting claim 24. Furthermore, Banno discloses:

A microprocessor according to claim 17, wherein said delay circuit comprises a shift register synchronized with the operations for the selection of said associated register (column 4 line 47 – column 5 line 61).

Claim 35 is rejected as applied above in rejecting claim 34. Furthermore, Banno discloses:

A microprocessor according to claim 16, wherein said second means comprises:

a delay circuit (Figure 2 item 12 c, column 4 line 47 – column 5 line 61);

a two-input AND logic gate having a first input connected to the output of said address decoder for selecting the register associated with said protection circuit, a second input connected through said delay circuit to the output of said second flip-flop circuit of first means, and an output connected to the selection input of said associated register (Figure 2 item 12c).

Claim 36 is rejected as applied above in rejecting claim 35. Furthermore, Banno discloses:

A microprocessor according to claim 17, wherein said delay circuit comprises a shift register synchronized with the operations for the selection of said associated register (column 4 line 47 – column 5 line 61).

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kaveh Abrishamkar whose telephone number is 571-272-3786. The examiner can normally be reached on Monday thru Friday 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ayaz Sheikh can be reached on 571-272-3795. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KA
04/28/05

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